Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-6 (canceled)

7. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming third gates on a first insulator film disposed on the silicon substrate ~~through a second insulator film~~; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a ~~first~~ second insulator film covering the third gates; a step of forming a first pattern to act as floating first gates in gaps formed between the third gates ~~through the first insulator film~~; and a step of forming control second gates on the upper surfaces of the floating first gates and the third gates, the height of the upper surfaces of the third gates thus formed being made lower than that of the upper surface of the first pattern, wherein

(a) in the step of forming the third gates, a plurality of third gates are formed in a stripe shape and are formed parallel to each other;

(b) in the step of forming the second conduction type semiconductor regions, the second conduction type semiconductor regions are formed on the well surface under one end of the third gates by tilted ion implantation using a plurality of stripe-shaped third gates as a mask; and

(c) the step of forming the first pattern is conducted after the step of forming the second conduction type semiconductor regions.

8. (original) A process according to Claim 7, wherein the first pattern is formed by any one of a first method of forming a polysilicon film to completely fill the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching; a third method of forming a polysilicon film so as not to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, a fourth method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film, and a fifth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps and polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing.

9. (currently amended) A process according to ~~any one of Claims 1-5,~~ Claim 7[[,]] or 8, wherein the third gates are self-aligned to the floating gates.

10. (currently amended) A process according to ~~any one of Claims 1-5,~~ Claim 7[[,]] or 8, wherein the floating gates are self-aligned to the third gates.

11-24. (canceled)

25. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device, which comprises

a step of forming a first conduction type well in a silicon substrate,

a step of forming a plurality of third gates ~~through a second insulator film~~ on a first insulator film disposed on the ~~semiconductor~~ silicon substrate,

a step of forming second conduction type semiconductor regions to act as sources/drains in the well,

a step of forming a ~~first~~ second insulator film covering at least side faces of the third gates and the ~~semiconductor~~ silicon substrate surface between ~~each~~ neighboring third ~~gate~~ gates,

a step of forming a first pattern which is to become floating first gates in individual gaps formed ~~by~~ between the third gates so as to make individual side faces of the first pattern opposed to side faces of neighboring third gates through the ~~first~~ second insulator film and to make a bottom side of the first pattern opposed to a surface of the ~~semiconductor~~ silicon substrate through the ~~first~~ second insulator film by depositing a floating first gate material film, followed by removing the material film above each third gate, and

a step of forming the floating first gates and forming control second gates on the third gates, wherein

(a) in the step of forming the third gates, a plurality of third gates are formed in a stripe shape and are formed parallel to each other;

(b) in the step of forming the second conduction type semiconductor regions, the second conduction type semiconductor regions are formed on the well surface under one end of the third gates by tilted ion implantation using a plurality of stripe-shaped third gates as a mask, and

(c) the step of forming the first pattern is conducted after the step of forming the second conduction type semiconductor regions.

26. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to claim 25, wherein the upper ends of side faces of the third gates are formed lower than the upper end side face of the first pattern which is to become the floating gates opposed to the side faces of the third gates.

27. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film for completely filling the gaps, and dry etching the polycrystalline silicon film.

28. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film for completely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, followed by dry etching.

29. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as to not completely fill the gaps, and polishing the polycrystalline silicon film by a chemical mechanical polishing method.

30. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as to not completely fill the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and polycrystalline silicon film to dry etching.

31. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, depositing a silicon oxide film for filling the gaps, and polishing the silicon film and the polycrystalline silicon film by a chemical mechanical polishing method.

32. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to any one of claims ~~14-21, 23, or 25-31~~ 25 to 31, wherein the third gates are formed as self-aligned to the floating gates.

33. (currently amended) A process for producing a nonvolatile semiconductor ~~integrated circuit~~ memory device according to any one of claims 1~~4-21, 23, or 25-31~~ 25 to 31, wherein the floating gates are formed as self-aligned to the third gates.

34-46 (canceled)

Amendments t the Drawings:

The attached drawing sheet contains a proposed revised version of FIG. 10(c), in which numeral 215 has been added to designate the appropriate element referenced in the specification.